REMARKS

The Examiner's Action mailed on March 2, 2006, has been received and its contents carefully considered.

In this Amendment, Applicants have amended claims 5 and 26, canceled claims 33 and 34, and added claims 35 and 36. Claims 5 and 26 are the independent claims, and claims 2-6, 9-10, 16-20, 26-32, 35 and 36 are pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Initially, it is noted that the Office Action summary indicates that claims 9, 10 and 32 have been objected to. However, Applicants have studied the Office Action, and have been unable to find any objections directed to these claims.

The Examiner has rejected claims 2, 4, 5, 17, 19 and 29 as being anticipated by *Zhang et al.* (USP 6,255,705). It is submitted that these claims are *prima facie* patentably distinguishable over the cited reference for at least the following reasons.

Applicants' independent claim 5 is directed to a semiconductor apparatus which includes a semiconductor substrate having an integrated circuit formed therein. A semiconductor thin film is bonded on a planarized region which is defined on a surface of the semiconductor substrate, and a planarized film is disposed between the planarized region and the semiconductor thin film. This invention has the advantages discussed in Applicants' specification, and is neither disclosed nor suggested by the cited reference.

Zhang et al. is directed to a device having both active matrix display circuits and peripheral circuits on the same substrate. The Examiner's Action has relied on the embodiment shown in Figures 1e and 3b in establishing his anticipation rejection. In particular, the Examiner's Action has equated the TFTs 151, 152 and 153 as being the equivalent of Applicants' claimed integrated circuit, and the lower layer film 102 as being the equivalent of Applicants' claimed planarized film. However, it is initially noted that the TFTs 151, 152 and 153 are formed over the substrate 101, and separated therefrom by the film 102, so that this reference does not disclose or suggest a semiconductor substrate having an integrated circuit formed therein, as recited by claim 5.

Moreover, the Examiner's Action has equated the surface of the semiconductor substrate as being a planarized region. However, the surface of the semiconductor substrate 102 is disposed underneath the TFTs 151, 152 and 153, whereas Applicants' claimed invention precludes this configuration, since the integrated circuit must be below the surface of the substrate, in order to be within the substrate.

Moreover, Applicants' claim 5 recites that the semiconductor thin film is bonded on the planarized region. The Examiner's Action has equated the active layers 125, 126 and 127 as being a semiconductor thin film. However, these features form a component of the TFTs 151, 152 and 153, and, in fact, form a lowermost portion of these components. Thus, these so-called semiconductor

thin films are not bonded on a planarized region, as recited by Applicants' independent claim 5.

Additionally, Applicants' claim 5 recites that a planarized film is disposed between the planarized region, and the semiconductor thin film. As noted above, the Examiner's Action has equated the film 102 as being a planarized film. However, this "planarized film" 102 is not between a planarized region and a semiconductor thin film, which is over an integrated circuit, as recited by claim 5. As such, it is submitted that Applicants' independent claim 5, and the claims dependent therefrom, have not been anticipated by the cited reference. It is thus requested that these rejections be withdrawn and that these claims be allowed.

The Examiner's Action has rejected claims 3, 6, 18, 26, 30 and 31 as being obvious over *Zhang et al.* in view of *Walker et al.* (USP 6,841,813). It is submitted that these claims are *prima facie* patentably distinguishable over the cited combination of references for at least the following reasons.

Initially, it is noted that *Walker et al.* do not overcome the above-noted deficiencies of *Zhang et al.* In particular, *Walker et al.* disclose a three-dimensional semiconductor apparatus that includes a plurality of semiconductor device layers. This reference teaches that each of the semiconductor device layers is formed on an entire upper surface of a layer over a substrate. However, this reference does not overcome the features deficient in *Zhang et al.*, as discussed above. Thus, dependent claim 3, 6, and 18 are submitted to be *prima facie* patentably distinguishable over the cited combination of references for at

least the same reasons as independent claim 5, from which these claims depend, as well as for the additional features recited therein.

Moreover, independent claim 26 is submitted to be *prima facie* patentably distinguishable over the cited references for reasons similar to independent claim 5. That is, the cited references do not disclose or suggest a planarized region that is defined on a surface of a semiconductor substrate with an integrated circuit being within the substrate, nor a semiconductor thin film which is bonded on the planarized region, with the semiconductor thin film being above the integrated circuit, as recited by claim 26. Additionally, *Walker et al.* fail to disclose or suggest a semiconductor thin film bonded on planarized region and another semiconductor thin film bonded on an upper surface of a raised layer, as recited by claim 26. Stated alternatively, none of the cited references disclose or suggest two kinds of semiconductor films, that is, a semiconductor thin film including at least one semiconductor device bonded on a planarized region, and another semiconductor thin film bonded on an upper surface of a raised layer, nor a planarized region and a raised layer having different heights, as recited by claim 26. As such, it is submitted that independent claim 26, and the claims dependent therefrom, are *prima facie* patentably distinguishable over the cited combination of references. It is requested that these claims be allowed and that these rejections be withdrawn.

The Examiner has also rejected claim 16 as being obvious over *Zhang et al.* in view of *Yamazaki et al.* (USP 6,184,556), and claim 20 as being obvious over *Zhang et al.* in view of *Hayashi et al.* (JP 09045930). Because either

Yamazaki et al. nor *Hayashi et al.* overcome the above noted deficiencies of *Zhang et al.*, it is submitted that claims 16 and 20 are *prima facie* patentably distinguishable over the cited references for at least the same reasons as independent claim 5, from which these claims depend, as well as for the additional features recited therein. It is requested that these claims be allowed and that these rejections be withdrawn.

The Examiner's Action has also rejected independent claims 5, and 26, and dependent claims 9 and 10 as being obvious over *Zhang* (US 2003/0067043) in view of *Muto et al.* (JP 61102767). It is submitted that these claims are *prima facie* patentably distinguishable over the cited references for at least the following reasons.

Initially, it is noted that it is difficult to ascertain which features of the *Zhang* reference the Examiner is equating to be the equivalent of Applicants' claimed features. For example, the Examiner relies on Figures 9 and 10BA in establishing his obviousness-type rejection. However, *Zhang* has similar deficiencies to those discussed above with respect to *Zhang et al.*, in that this reference does not disclose or suggest a combined semiconductor apparatus which includes a semiconductor substrate having an integrated circuit formed therein, with a planarized region being defined on a surface of the semiconductor substrate, and a semiconductor thin film which includes at least one semiconductor device being bonded to the planarized region, and a planarized film disposed between the planarized region and the semiconductor thin film, all as recited by independent

claim 5. Similarly, this reference does not disclose or suggest the features recited within claim 26, which include the semiconductor thin film including at least one semiconductor device being bonded to the planarized region which is defined in a surface of a semiconductor substrate. Similarly, *Muto et al.* do not overcome the above noted deficiencies of *Zhang.* As such, it is submitted that Applicants' independent claims 5 and 26, and the claims dependent therefrom, are *prima facie* patentably distinguishable over the cited combination of references. It is requested that these claims be allowed and that these rejections be withdrawn.

The Examiner's Action has also rejected claims 27, 28, 33 and 34 as being obvious over *Zhang et al.* and *Walker et al.*, and further in view *Hayashi et al.*, and has rejected claim 32 as being obvious over *Zhang* and *Muto et al.*, and further in view of *Puar* (USP 4,342,102). Because these secondary references do not overcome the deficiencies of the primary references, it is submitted that these dependent claims are *prima facie* patentably distinguishable over the cited combination of references for at least the same reasons as independent claim 26, as well as for the additional features recited therein. It is requested that these claims be allowed and that these rejections be withdrawn.

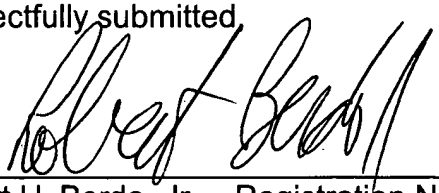
The Examiner has rejected claims 33 and 34 as being duplicates of claims 27 and 28. Because these claims have been canceled, these rejections have been rendered moot.

It is submitted that this application is now in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should any fee be required, the Commissionaire is hereby authorized to charge the fee to our deposit account No. 18-0002, and notify us accordingly.

Respectfully submitted,



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Date

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